MODEL 2600 LR
LTC READER

INSTRUCTION MANUAL

January, 1984

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MODEL 2600 LR
LTC READER

TABLE OF CONTENTS

Model 2600 LR

LTC Reader

1. Description

1.1 Introduction

The Model 2600 LR LTC Reader accepts longitudinal time code (LTC) and, if desired, either control track and direction signals from video tape recorders (VTRs) or tachometer and direction signals from audio tape recorders (ATRs), all at tape speeds from 1/20 to 100 times play speed. The control track/tach signals can be used to update the time code count whenever the LTC becomes unreliable or, on ATRs, when the tape lifters operate. If direction signals are not available, the 2600 LR can be instructed to learn the last known tape direction from the LTC and to update in that direction until new LTC appears.

An ATR lifter control output is provided which permits any of three modes of lifter operation to be selected by the user. The output can be programmed to defeat the lifters at all times (to permit time code to be recovered at all tape speeds); to allow the lifters to operate at tape speeds above two times play speed (normal operation); or to implement a sample mode. In the sample mode, the lifters operate normally, but are forced to return the tape to the heads occasionally to allow the reader to sample the time code.

When the lifter control output is not connected to an ATR, no lifter control is exercised by the reader. In this situation, tach pulse updating may occur even at slow tape speeds, because some recorders only allow the tape to touch the heads during Play.

When the lifters of an ATR are defeated at all times, allowing time code to be read at all tape speeds (for instance, to handle discontinuous time code), the playback amplifier associated with the ATR's time code track must be wide-banded (bandwidth about 150 KHz) in order to handle the high frequency rectangular waveforms of the time code. Whether or not the playback amplifier is wide-banded, it should have good low frequency response to permit the code to be read at low speeds (while tape is starting and stopping). Some ATR manufacturers supply special wide-band SMPTE/EBU time code amplifiers for their transports.

The reader supplies, on the data bus, decoded longitudinal time code or time code updated by control track or tach pulses, in that order of priority, switching automatically if the LTC proves unreliable. The data bus signals are always compensated for decoding delay by adding one to each reading.

When available, all other decoded information, such as user bits, color frame flag, drop frame flag (NTSC only), and the binary group flags (which can be used to indicate how the user bits should be decoded), is also supplied on the bus. Error bypass routines are used so that occasional drop-outs or incorrect codes will not effect the recovered time code sequence.

NOTE

See Section 1.1 of the Model 2600 LG LTC Generator manual for information about how the binary group flags should be interpreted.

The front panel digital display can be frozen when desired, either from the front panel or by a remote switch, without interrupting data bus flow.

If the data in the user bits is time code which forms a consistant counting sequence, then the reader can be set to compensate the user bits data for decoding delay.

Both sliced LTC and input code rate frame edge sync pulses (extracted from the sync word of the LTC) are available at the rear panel. The sync pulses can also be distributed to other modules over the data bus.

1.2 Inputs and Outputs

All of the external input and output connections are made through connectors on the rear of the module. The mating plugs for the common connectors used (BNC and XLR-type audio plugs) are not supplied since they are readily available in all studios. The mating plugs for all other connectors are supplied with the module.

1.2.1 Time Code Input

One TC IN XLR-3F jack accepts a 50 mV to 10 Vpp longitudinal time code signal. Impedence is 10K ohms, differential; rate may be 1/20th play speed to 100 times play speed. Connections are:

Pin 1: signal ground
Pin 2 and Pin 3: differential input
Shell: chassis ground

1.2.2 Time Code Output

One SLC OUT XLR-3M jack provides a single-ended TTL-level longitudinal time code output with waveshape improved by slicing. Connections are:

Pin 1: Signal ground
Pin 2: Signal ground
Pin 3: LTC out
Shell: Chassis ground

1.2.3 Remote Freeze Control

One REM FREEZE BNC jack accepts an input to freeze the display when desired. The freeze signal can be either a continuous contact closure to ground or a low TTL level.

1.2.4 Sync Output

One SYNC WD OUT BNC jack provides a TTL-level positive pulse output of one LTC bit duration, synchronized to the received longitudinal time code sync word. The leading edge is coincident with the frame edge of the LTC.

NOTE

The sync signal is only generated when valid LTC is being received and decoded; it is not generated when the reader is updating from control track/tach pulses.

1.2.5 Transport Connector

One TRANSPORT connector, Amphenol type 57, 14-pin female, provides for the input and output signals to and from a VTR or ATR. Mating plug is Amphenol 57-30140. The signals are:

Pin 1: DC-coupled TTL-level control track/tach input. Rates from 1/20 to 100 times play speed, with number of pulses per second (at play speed) from 1 to 255 selectable internally by DIP switches.

Pin 2: tape direction input. TTL logic levels or contact closure to ground, with sense selectable internally by jumper.

Pin 3: AC-coupled non-TTL-amplitude control track/tach input. Accepts 1/2 V to 2 1/2 V peak pulses of either polarity, with base line between -12 and +12 VDC, and supplies, on pins 8 and 9, amplified waveforms suitable for connection to pin 1.

NOTE

If number of pulses per second (at play speed), amplitude, baseline level, polarity and width of pulses and levels, and sense of tape direction signal are not known, then oscilloscope observations should be made.

Pin 4: sliced LTC output. Same as pin 3 of SLC OUT connector.

Pin5/Pin 6: differential LTC input, Same as TC IN connector, pins 2 and 3.

Pin 7: logic ground.

Pin 8: amplified pin 3 output. Connect to pin 1 to count positive excursions of pin 3 input

Pin 9: amplified pin 3 output. Connect to pin 1 to count negative excursions of pin 3 input.

Pin 10/Pin 11: lifter control output. Provides relay closure between pins or an open collection-open emitter transistor switch sinking current from pin 11 (collector) to pin 10 (emitter) when lifter defeat is called for. Type of output is selected by jumpers.

Saturated transistor switch rating:
Current: 10 ma, max.
Pin 11 voltage: +15 VDC, max.
Pin 10 voltage range: +1 to -15 VDC, max.

Relay contact rating:
Current: 1 amp, max.
Voltage: 28 VDC, max.

Pin 12: -12 VDC output, less than 20 ma load.

Pin 13: +12 VDC output, less than 20 ma load.

Pin 14: +5 VDC output, less than 100 ma load.

1.3 Controls and Indicators

All of the external controls and indicators of the module are located on the front panel.

TIME: interlocked pushbutton used to enable display of time.

UBITS: interlocked pushbutton used to enable display of user bits.

NOTE

When both TIME and UBITS pushbuttons are disabled (by gently pushing the buttons as necessary to trip both to OUT position), decimal display will show user-selected address of module.

FREEZE: alternate-action pushbutton used to freeze display without interrupting data bus operation.

COMP UB: alternate-action pushbutton used to enable user bits compensation.

CT/T: LED lights when time code is being updated by control track or tach pulses.

DF: LED lights when drop-frame bit of time code being received is set to one.

CF: LED lights when color frame bit of time code being received is set to one.

Numeric Display: eight-digit decimal display of time, user bits or module address.

1.4 Computer Interfacing

Communications between the LTC Reader and external computer equipment can be carried out over the data bus through a Serial Interface module. The interface can accept data which the reader broadcasts on the bus, and send it to the external equipment when instructed to do so. Additionally, a Parallel Interface can be used to output data to external equipment.

The message protocols which apply to the LTC Reader are listed in Section 3.4. For a complete description of communications operation, refer to the Model 2600 SI Serial Interface section of this manual. The LTC Reader constitutes a single device for interfacing purposes.

2. Set-Up and Adjustment

Two printed circuit boards (PCBs) are used in the LTC Reader module. The Longitudinal Reader PCB is the left-hand board as viewed from the front of the module; the LR Processor PCB is the right-hand board.

The PCBs contain controls and jumpers which must be adjusted and positioned to set up the module to match the system in which it is to be installed. Many, but not all, of the controls and jumpers are located along the top edges of the PCBs, and most are identified by etch marking on the boards. However, positive identification should be made by referring to the assembly drawings in Section 5.

The potentiomenters, rotary switches, DIP switches and capacitors are of conventional design for PCB use and are readily identifiable. The jumpers are small, blue-insulation-covered, rectangular, box-shaped metal plugs which connect together pairs of adjacent metal pins. They are held in place by friction. Very occasionally, a jumper is an actual piece of wire soldered between two etch pads. The factory settings of jumpers for shipment are indicated by asterisks (*).

Only those controls and jumpers used in system set-up are described in this section. There are others on the PCBs which are for use by service personnel, and these are described in Section 4, Test and Trouble-Shooting. Finally, there are some controls and jumpers for use only by factory personnel during manufacture; these are not described and should not be disturbed.

2.1 Longitudinal Reader PCB

S1: 8-position DIP switch (all positions used). Entire switch is used to generate a binary number from 0 to 255, corresponding to number of play speed pulses per second of control track/tach input signal. B1 is LSB, B8 is MSB. ON sets a bit to one. All switches OFF defaults to frame rate.

NOTE

The relationship between the DIP switch positions and the binary numbers is:

B8	B7	B6	B5	B4	B3	B2	B1
128	64	32	16	8	4	2	1

To set a pulse rate, turn on the switches necessary to make the associated binary numbers add up to the desired rate. For instance, to set a tach rate of 30 pps, turn on switches B5, B4, B3 and B2 (16 + 8 + 4 + 2 = 30).

R8: multi-turn pot adjusts input voltage range of LTC input. Set so signals below 50 mV are ignored.

R9: multi-turn pot adjusts demodulator clock to 10 MHz.

JP2/JP3: Two 2-position jumpers select the type of signal output (between pins 10 and 11 of TRANSPORT connector) to be used for defeating audio tape recorder (ATR) tape lifters. The two jumper positions R* select relay closure output. The two jumper positions L select saturated transistor switch output.

2.2 LR Processor PCB

S4: 10-position rotary switch defines numeric address of this module. Set switch to a unique number within the system.

S3: 8-position DIP switch (4 positions used).

B1: ON allows ATR tape lifters to operate normally at tape speeds greater than two times play speed.

NOTE

When B1 is OFF, lifters are defeated at all times.

B2: ON forces ATR tape lifters to return tape to heads occasionally (approximately one second out of every four), allowing reader to sample time code.

NOTE

B1 must be ON when B2 is ON. Otherwise, lifters will be defeated at all times.

B3: not used.

B4: ON forces processor to use 24-frame standard, with B5 OFF.

B5: ON forces processor to use 25-frame standard, with B4 OFF.

B4 and B5 ON together forces processor to use 30-frame standard.

B4 and B5 OFF together allows processor to use system standard, if available from LTC Generator. If system standard is not available, default is to 30-frame standard.

NOTE

System standard is set by LTC Generator only if its address is zero.

B8: ON instructs processor to use last known time code direction when updating from control track/tach pulses.

JP5: Permits LTC Reader to drive the AUXV (bus line 28) data bus line with whatever output is on its SYNC WD OUT connector.

JP6: 2-position jumper selects the logic sense of the direction input at pin 2 of TRANSPORT connector. In FWL (ForWard Low) jumper position, low logic level or closure to ground causes counter to count up. In RVL* (ReVerse Low) jumper position, low logic level or closure to ground causes counter to count down.

NOTE

If logic levels for forward and rewind are not known, oscilloscope observations should be made.

3. Operation

Prior to beginning operation, the appropriate rear panel input and output connections must be made, and the internal controls and connections must be set up to accomodate the system in which the reader is installed. The front panel controls must be set to compensate user bits, if appropriate, and to select the data to be displayed.

Normally, no controls need be manipulated during operations.

3.1 LTC Connections

Longitudinal time code connections to and from the module should be made with shielded, twisted-pair audio cable using type XLR-3 audio connectors. Alternatively, the input time code can be supplied to the module through pins 5 and 6, and the output taken from pin 4, of the TRANSPORT connector.

3.2 Transport Connections

If control track pulses (from VTRs) or tach pulses (from ATRs) are to be used to update time code reading in the absence of recoverable time code, then the appropriate signals from the recorder must be connected to the TRANSPORT connector and the internal jumpers connected as explained in Sections 1.2.5 and 2.2. If non-TTL-amplitude control track/tach pulses are to be used, they should be fed to pin 3 of the transport connector, and then either pin 8 or pin 9 should be connected to pin 1.

NOTE

Control track/tach pulse updating cannot be used successfully if discontinuous time code is in use.

The lifter control output must be connected and enabled if this function is to be used.

3.3 Internal Set-Up

Refer to Sections 2.1 and 2.2 for detailed information regarding the internal set-up controls. Normally, these controls will not need to be reset once a system is in operation.

On the Longitudinal Reader PCB, calibration adjustment pots R8 and R9 should not need attention unless system levels change dramatically.

DIP switch S1 must be set to correspond to the number of pulses per second (at play speed) generated by the ATR or VTR with which the reader is to be used.

NOTE

If number of pulses per second (at play speed) is not known, oscilloscope observations of recorder control track/tach output should be made.

Jumpers JP2 and JP3 will only need attention if transistor switching, instead of relay switching, of the tape lifters is to be implemented.

On the LR Processor PCB, S4 should be set to define the numeric address of the module.

Jumper JP5 should be put in the AUXV position if the module's SYNC WD OUT signal is to be distributed on bus line 28.

Jumper JP6 should be changed if necessary to match the recorder's direction signal output.

When the module is to be used with an ATR, bits 1 and 2 of S3 should be set to match the type of operation desired. Bit 8 should be set if the transport does not have a direction signal, and if tach pulse updating is to be used. Bits 4 and 5 should be set to match the system standard, if a standard is not imposed by an LTC Generator.

3.4 Message Protocols

No commands or data can be received by the LTC Reader over the data bus. Since the LTC Reader always broadcasts its data on the data bus when it becomes available, the data may be transmitted to external communications equipment by a Model 2600 SI Serial Interface. A full description of interface operation is contained in the Model 2600 SI Serial Interface section of this manual. The message protocols listed below are those associated with the LTC Reader. The ASCII hex codes, as well as the characters themselves, are listed below for the purpose of absolutely defining each character.

CHARACTER	ASCII HEX CODE	COMMAND

Establishing Communication

#	23	Call-up character, indicating that the character which follows is a module address.

Sending data:

$	24	Dual function command calls up Model 2600 SI Serial Interface module and instructs it to be ready to collect and send data from module most recently called up.

NOTE

Once a $ character has been sent to the Serial Interface (to call it up), data and commands can not be sent to any other module until that module has been called up again.

T 54 Send data in Time register. Format is:

A $\overline{SP}$ H H : M M : S S : F F $\overline{CR}$ $\overline{LF}$

where A = module address
$\overline{SP}$ = space
H = hours
: = colon
M = minutes
S = seconds
F = frames
$\overline{CR}$ = carriage return
$\overline{LF}$ = line feed

U 55 Send data in User-bits register. Format is:

A $\overline{SP}$ D D $\overline{SP}$ D D $\overline{SP}$ D D $\overline{SP}$ D D $\overline{CR}$ $\overline{LF}$

where D = any four-bit hexadecimal character

S 53 Send data in Status-bits register. Format is:

A $\overline{SP}$ I G , F F . 0 0 , 0 0 $\overline{CR}$ $\overline{LF}$

where I = a frame identification character, as follows:

MODE	CHARACTERS
24	E
24 CF	A, B
25	A, B
25 CF	A, B, C, D
30	E
30 CF	A, B
30 DF	E
30 DF CF	A, B
CT/T	C

NOTE

In all modes, frame identification character is C when reader is updating from control track or tach pulses.

G = a four-bit hexadecimal character in which the four bits are interpreted individually as follows:

B4 (MSB) = color frame flag
B3 = drop frame flag
B2 = binary group flag (lower bit in code)
B1 = binary group flag (higher bit in code)

. = decimal point

F = reserved digit

0 = unused digit

I 49 Iterate (continue to send) data indicated by last command, at baud rate.

Q 51 Quit (stop) sending data.

NOTE

The Model 2600 SI Serial Interface can be instructed to send data continuously from a module while new data and commands are sent to the same or to other modules.

3.5 Hexadecimal Numbers

Unlike decimal numbers, which have ten values (the digits 0 through 9), hexadecimal numbers have 16 values (the digits 0 through 9 and the letters A through F). They are convenient to use in programming because the 16 values permit all possible states of a four-bit binary number to be defined, while at the same time permitting the value to be displayed on a single-character digital display. The hexadecimal numbers, their binary equivalents, and their decimal equivalents, are:

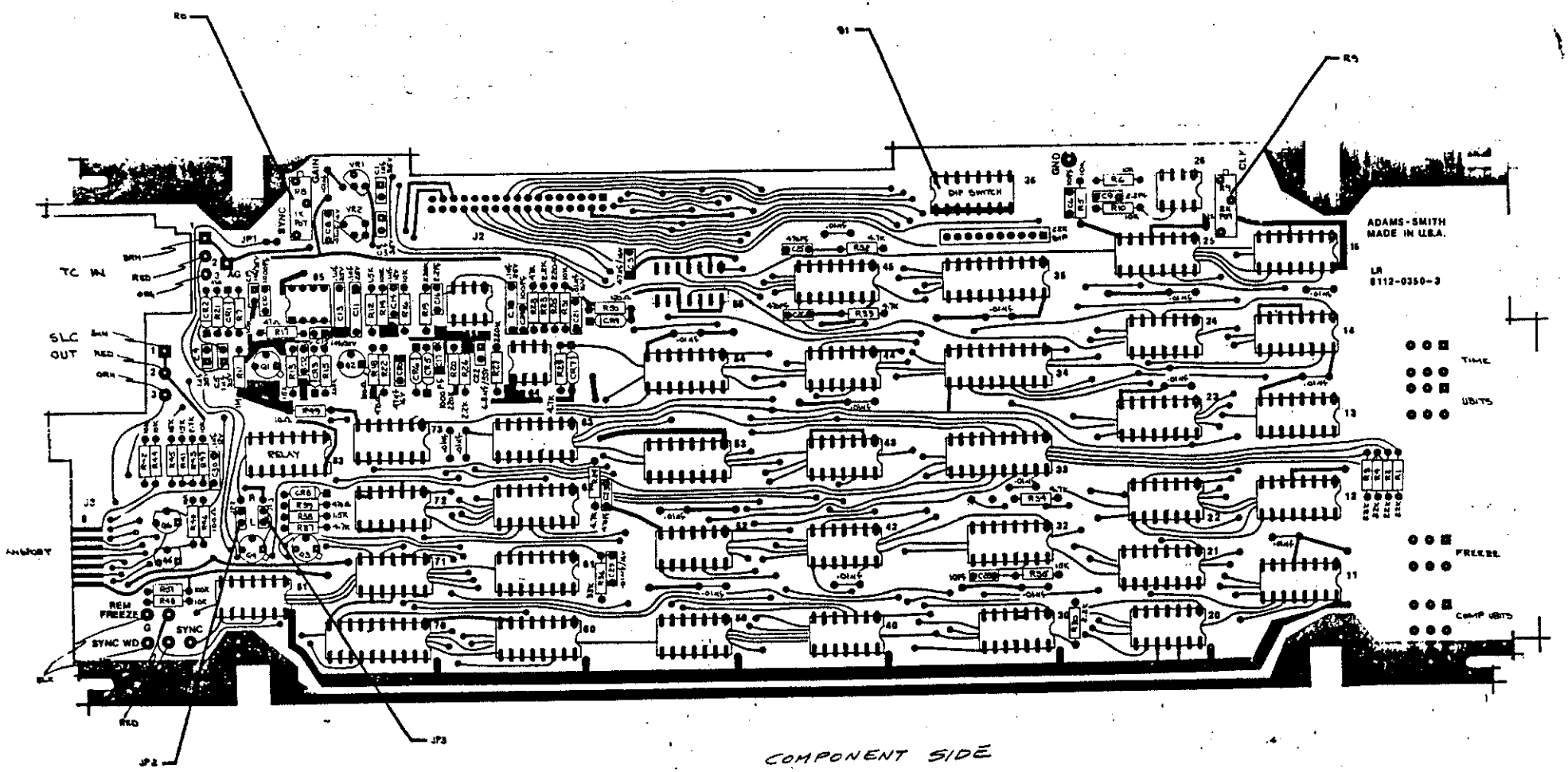
HEXADECIMAL NUMBER	BINARY EQUIVALENT	DECIMAL EQUIVALENT
0	0 0 0 0	0
1	0 0 0 1	1
2	0 0 1 0	2
3	0 0 1 1	3
4	0 1 0 0	4
5	0 1 0 1	5
6	0 1 1 0	6
7	0 1 1 1	7
8	1 0 0 0	8
9	1 0 0 1	9
A	1 0 1 0	10
B	1 0 1 1	11
C	1 1 0 0	12
D	1 1 0 1	13
E	1 1 1 0	14
F	1 1 1 1	15

The decimal equivalent of a hexadecimal number can be determined by writing the binary equivalent and then summing the weighted values of the ones in the binary number. For instance, the decimal equivalent of the single hexadecimal character D is determined as follows:

HEX NUMBER	D			
BINARY EQUIVALENT	1	1	0	1
BINARY BIT WEIGHTS	8	4	2	1
SUM OF WEIGHTED ONES	8 +	4 +	0 +	1 = 13

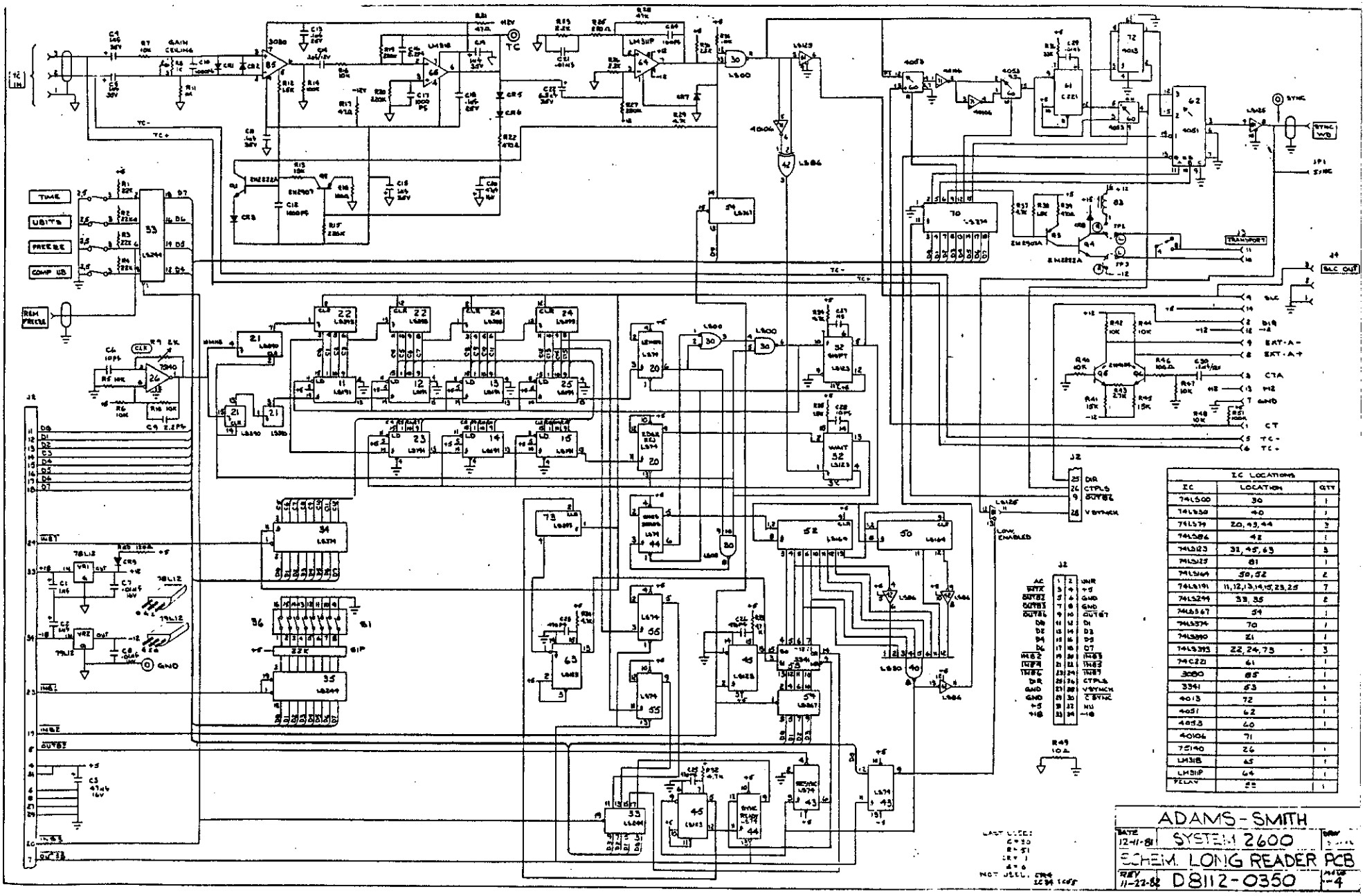
The decimal equivalent of a multi-character hexadecimal number can be found by writing the binary equivalents of the characters as a single binary number and then summing the weighted values. For instance, the decimal equivalent of the hexadecimal number 5C is 92, determined as follows:

HEX NUMBER		5				C			
BINARY EQUIVALENTS	0	1	0	1	1	1	0	0	
BINARY BIT WEIGHTS	128	64	32	16	8	4	2	1	
SUM OF WEIGHTED ONES	0	+ 64	+ 0	+ 16	+ 8	+ 4	+ 0	+ 0	= 92



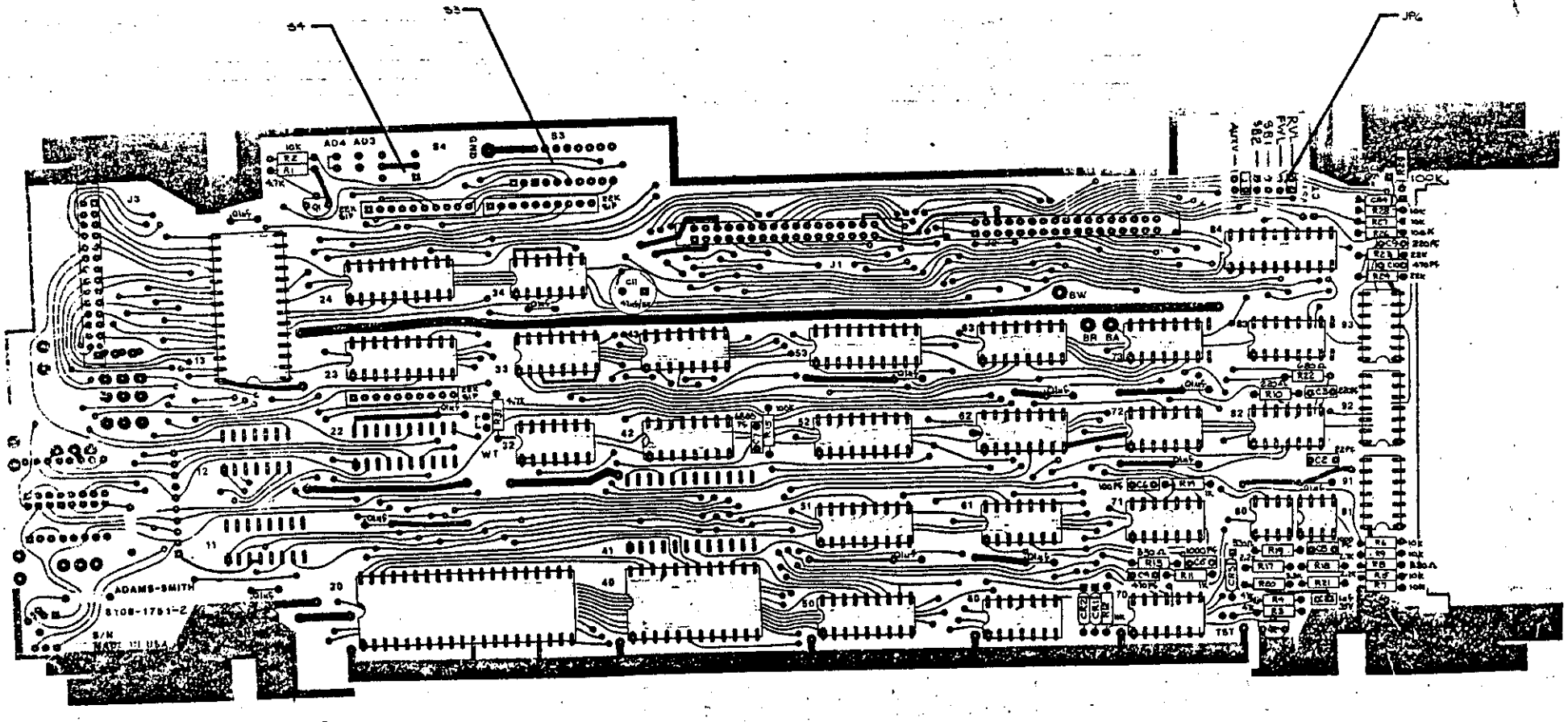
COMPONENT SIDE

ADAMS·SMITH		
	SYSTEM 2600	
ASSEMBLY LONG READER PCB		
ATE 2-29-82	D8211-0453	ASS. NO 3



IC LOCATIONS		
IC	LOCATION	QTY
74LS00	30	1
74LS30	40	1
74LS74	20, 43, 44	3
74LS86	42	1
74LS123	31, 45, 63	3
74LS125	61	1
74LS244	50, 52	2
74LS191	11, 12, 13, 14, 15, 23, 25	7
74LS244	33, 35	2
74LS367	54	1
74LS374	70	1
74LS390	21	1
74LS393	22, 24, 73	3
74C221	61	1
3080	85	1
3341	63	1
4013	72	1
4051	62	1
4053	60	1
40106	71	1
75140	26	1
LM318	65	1
LM319	64	1
RELAY	55	1

ADAMS - SMITH		
DATE 12-11-81	SYSTEM 2600	DRAWN
SCHEM. LONG READER PCB		
REV 11-22-82	D8112-0350	SHEET -4



FRONT

ADAMS·SMITH		
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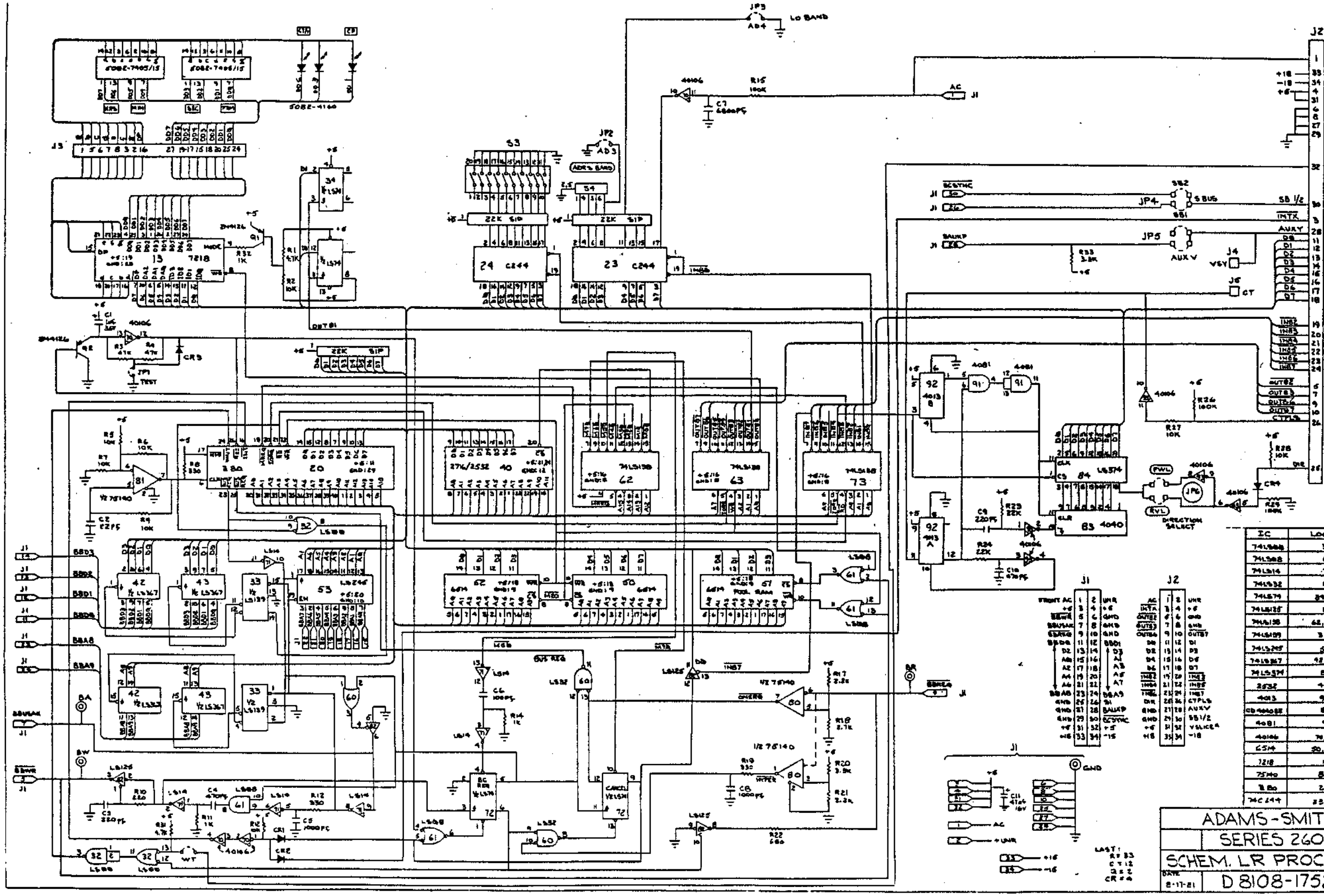
ASSEMBLY	PROCESSOR PCB	
DATE 9-22-82	D8... 0454	PSS. NO 3 5.225-01



IC	LOCATION	QTY
74LS00	52	1
74LS08	61	1
74LS14	71	1
74LS32	60	1
74LS74	34,72	2
74LS125	82	1
74LS138	62,63,73	3
74LS139	33	1
74LS245	53	1
74LS367	42,43	2
74LS374	84	1
2532	40	1
4013	92	1
CD4040BE	83	1
4081	91	1
40106	70,93	2
6514	50,51,52	3
7218	13	1
75140	80,81	2
Z80	20	1
74C244	23,24	2

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SERIES 2600

SCHEM. LR PROCESSOR PCB

DATE 8-17-81

D 8108-1752

REVISED 10-23-8

FIELD BULLETIN

ADAMS•SMITH

Model 2600 LR

Field Bulletin LR-2
Software Version LR-C

Date: August 20, 1986

To: Users of Model 2600 LR LTC Reader

SOFTWARE UPDATE

New software routines have been introduced in this level of software, "C" Software, to increase the performance of the System 2600 LR Longitudinal Time Code Reader. The implementation of C software requires the replacement of the PROM on the LR Processor PCB and the addition of a 3.3K-ohm resistor as shown in Figure LR-2-1. The sum check of the new "C"-level PROM is D956.

Please note that all dipswitch-selectable routines, and new Serial Communications Protocols are listed at the end of this bulletin. Keep this bulletin with your System 2600 manual for reference to the features which are provided by C-level software.

New features included in version C software are:

1) New LR Serial Communication Protocols have been added which allow commands and data to be sent to the LTC Reader via a Model 2600 SI Serial Interface module. Previously, it was possible to transmit LTC data from the LTC Reader via a 2600 SI Serial Interface module, but it was not possible to send commands or data to the LTC Reader via a 2600 SI module. The new commands are listed at the end of this bulletin.

2) The LTC Reader now has a tach and direction "learn" mode which allows the LTC Reader to automatically determine the tach rate of a transport at play speed and the sense of that transport's direction signal or tally. This feature eliminates the need to set Dipswitch S1 on the Longitudinal Reader PCB each time a different transport is connected to the LTC Reader.

   An advantage of the "learn" mode is that it can measure tach rates greater than 255 pulses per second (pps). When setting tach rate on Dipswitch S1, 255 pps is the maximum tach rate which can be entered. In addition,

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the "learn" mode is capable of measuring fractional tach rate (such as 8.25 pulses per second).

The LTC Reader will "learn" the tach rate and direction sense of a transport when dipswitch S3,B6 is ON and a tape containing known-good time code is played. The CT/T LED will flash until the tach rate and direction have been calculated. After calculation has been completed and the LTC Reader is being used in normal time code operation, the "learn" mode will 'fine tune' the calculation by using successive time code readings. The learning process will automatically re-start IF one of the following occurs:

a) Any significant change in tach rate (note that minor changes will be accommodated by the 'fine tuning' process).

b) A reversal of the sense of the direction signal.

c) A change in the setting of dipswitches S3,B4 and S3,B5 (time code frame rate).

d) Pressing of the FREEZE push-button. This action will only restart the learning process if dipswitch S3,B3 is ON (Refer to new Dipswitch routines) and time code is present on the tape.

NOTE

When the LTC Reader is first powered-up, the "learn" mode will default to the tach rate set on the Longitudinal Reader PCB Dipswitch (U36) before reading time code.

3) The tach rate which is currently being used by the LTC Reader will be displayed when both the TIME and UBITS buttons are pressed. Note that after power-up, this display will show all zeroes until tach activity is detected. The display is interpreted as follows:

HRS locations:	ØØ signifies no direction inversion with respect to the setting of jumper JP6.
	8Ø signifies direction sense is being inverted with respect to the setting of jumper JP6.
MIN and SEC locations:	Represents the integer part of the tach rate as a hexadecimal number. (MIN will usually be ØØ, unless the tach rate is

over 255 Hz. Note that 255 would be shown as FF in the SEC area.)

FRM locations: Represents the fractional part of the tach rate. The actual fraction is XX/256.

4) The lifter defeat routines have been augmented. These routines now allow more accurate time code reading during deceleration of the transport. In addition, the sampling mode has been modified to allow the tape to re-lift from the heads as soon as valid time code has been read, instead of being held against the heads for a fixed interval. This routine can be invoked by setting BOTH Dipswitches S3,B1 and S3,B2 to ON. (See new dipswitch routines)

5) The output of frame edge pulses on the System AUXV line (bus line 28) is now inhibited during high speed winding where time code is present. External computers (such as console automation systems) following the frame edge pulses will not try to follow at high speeds.

6) The LTC Reader now produces the frame rate information needed by the Translator Interface to generate LTC from over the bus addresses. Previously, only the VITC Reader was designed to supply this information to the Translator Interface.

DIPSWITCH ROUTINES

All functions invoked by the dipswitches on the Processor PCB are listed below.

SWITCH NUMBER	STATE OF SWITCH	DESCRIPTION
S3,B1 and S3,B2 operate as a pair to control lifter operation.		
S3,B1 S3,B2	OFF OFF	Lifters are always defeated.
S3,B1 S3,B2	ON OFF	Lifters are defeated only when transport is operating slower than two times play speed.
S3,B1 S3,B2	OFF ON	Lifters are never defeated.
S3,B1 S3,B2	ON ON	Lifters are defeated when transport is operating slower than two times

play speed. Also, time code is sampled when transport is operating at high speeds.

Modification of operation of front panel FREEZE switch.

S3,B3	ON	Modifies the function of the front panel FREEZE switch as follows: 1) When time code is present, pressing FREEZE will cause the 'tach learn' routines to re-learn the tach rate and direction sense IF the 'tach learn' routine is invoked by dipswitch S3,B6. 2) When no time code is present (using tach-only pseudo time code mode) pressing FREEZE will reset the current time code value to all zeros.
S3,B3	OFF	The front panel FREEZE switch operates as before, where pressing FREEZE will freeze the display of the LTC Reader without interrupting data bus operation.

Note that S3,B4 and S3,B5 operate as a pair to determine the time code standard to be used by the LTC Reader.

S3,B4 S3,B5	OFF OFF	The LTC Reader module will use the time code standard set by the module located at address 'Ø' on the data bus (which is convenient because the LTC Generator is usually set to address 'Ø'). If the LTC Reader is located at address 'Ø', then 3Ø frames per second becomes the system time code standard.
S3,B4 S3,B5	ON OFF	The time code standard used by the LTC Reader is 24 frames per second.
S3,B4 S3,B5	OFF ON	The time code standard used by the LTC Reader is 25 frames per second.

S3,B4 S3,B5	ON ON	The time code standard used by the LTC Reader is 30 frames per second.

Tach rate and direction sense "learn" mode.

S3,B6	ON	Tach and direction "learn" mode is invoked. The tach rate and direction sense of the transport will automatically be calculated when good time code is read. Note that the CT/T LED will blink until the calculation is finished.
S3,B6	OFF	Tach and direction "learn" mode is NOT invoked. Tach rate must be entered into dipswitch S1 and direction sense must be set by blue jumper JP6 on the LR Processor PCB.

S3,B7 and S3,B8 operate as a pair to ascertain tape direction from bi-phase signals for CTL/TACH updating.

S3,B7 S3,B8	OFF OFF	Direction sensed at all time from signal applied to direction input.
S3,B7 S3,B8	ON OFF	Direction sensed only from signal applied to direction input, and only when tape slows to a stop.
S3,B7 S3,B8	OFF ON	Direction learned only from direction of most recent valid time code, with signal at direction input ignored.
S3,B7 S3,B8	ON ON	Direction sensed both from signal applied to direction input when tape slows to a stop, and learned from valid time code.

NOTE

A special combination of dipswitch settings will disable the time-code-plus-1 testing. This feature prevents the LTC Reader from checking incoming time code for continuity, and allows time code with non-continuous numbers to be recognized. Note that

"non-continuous" does not mean "discontinuous". The feature is useful, for example, when a dubber has the capability of transmitting time code numbers -- but will only transmit the numbers in short bursts at high speeds.

The feature is invoked under the following condition:

S3,B6 ON
S3,B7 OFF
S3,B8 ON

NOTE that the usual functions associated with S3,B6 (tach learn) and S3,B8 (tach and direction sense from time code) are disabled.

SERIAL COMMUNICATIONS PROTOCOLS FOR THE LTC READER

The LTC Reader is now capable of receiving commands and data over the data bus from a Model 2600 SI Serial Interface module, by using the message protocols listed below. Data from the LTC Reader may be transmitted, as before, to external communications equipment, through use of previously published protocols.

NOTE

The format to be used to entering Serial Communication protocol is shown in brackets <>. The brackets only represent the format in which the information associated with the protocol should entered, the brackets themselves should not be entered. For example, X <Ø-F> indicates that "X" is to be used as a prefix before any of the numbers Ø-9, or A-F to allow these numbers to be interpreted as hexadecimal. The hexadecimal number "A" would be entered as "XA".

CHARACTER (ENTRY FORMAT SHOWN BY < >)	ASCII HEX CODE	COMMAND
Loading Data from External Equipment:		
<Ø-9>	3Ø-39	Numbers. Always appear first in the hundreths or right-hand-most position of the keyboard entry

		register, and then shift one position to the left as each new number is entered.
X <Ø-F>	58	Hexadecimal number prefix command. Allows the letters A-F (41-46) to be interpreted as hexadecimal numbers.
<_> (underscore) or BACKARROW	5F	Fills data entry register with zeros (same as entering a string of 1Ø zeros).
B	42	Blank data entry register.
CTRL H or DEL	Ø8 or 7F	Erase previously-entered digit to permit a different (corrected) digit to be entered (can only be used to delete numbers before a terminator has been sent).

System Control Commands:

CTRL K	ØB	Initiate power-up type reset.
<Ø or 1> CTRL L	ØC	Used as a terminator of a message to enable/disable the front panel control. When used after a 1 (entered 1 CTRL L), will lockout the use of the module's front panel. When used after a Ø (entered Ø CTRL L), will reinstate use of the module's front panel.
<Ø or 1> CTRL V	16	When used after a 1, will enable frame edge reference broadcasting on the AUXV bus (bus line 28). When used after a Ø, will disable frame edge reference broadcasting on the AUXV bus (bus line 28).
<2 digits> R	52	Overrides the dipswitch setting (of tach rate) on the LR PCB. The two digits which preceed the "R" represent the tach rate (in hexadecimal) which the user wishes to enter into the module.

<2 digits> S	53	When preceeded by two digits, overrides the dipswitch settings on the Processor PCB of the LTC Reader module. The module will accept the dipswitch setting (either software entered or manual setting of the dipswiches) which was entered most recently. The two digits preceeding the 'S' represent the hexadecimal equivalent of the binary ON/OFF positions of the individual dipswitches.
<8 digits> T	54	Used as a terminator when entering a starting time code for tach-only operation.
<Ø or 1> U	55	When preceeded by a 1, will enable UBITS compensation (the same as pressing the UBITS button on the front panel of the LTC Reader module). When preceeded by a Ø, will disable UBITS compensation (the same as releasing the UBITS button on the front panel of the module). Note that the module accepts the most recent command received (either use of the front panel button, or software command).